**PARUL UNIVERSITY - FACULTY OF ENGINEERING & TECHNOLOGY**

**Department of Electronics & Communication Engineering**

**ASSIGNMENT-1**

**Subject Name: DIGITAL ELECTRONICS**

**Subject Code: 203105201**

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1. Convert Decimal Number 250.5, 87.876 to base 3, base 4, base 7 & base 16.

2. Convert decimal number 225**.**225, 865.987 to binary, octal and hexadecimal.

3. Represent decimal number 7654 in BCD , Excess-3 , and Gray code

4. Convert following Numbers as directed: (a) (52)10 = ( )2

(b) (101001011)2 = ( )10 (c) (11101110) 2 = ( )8 (d) (68)10 = ( )16

5. Define: Digital System.

6. Convert following Hexadecimal Number to Decimal number : B28, FFF, F28

7. Convert following Octal Number to Hexadecimal and Binary number :

414, 574, 725.25

8. Convert following numbers to decimal number:

(i) (10001.101)2 (ii) (101011.11101)2 (iii) (0.365)8

(iv) A3E5 (v) CDA4 (vi) (11101.001)2 (vii) B2D4

9. Perform subtractions with the following binary numbers using 2′ s complement

(i) 10010 - 10011 (ii) 100 -110000 (iii) 11010 -10000

10.Perform subtractions with the following binary numbers using 1′ s complement

(i) 100110 - 10011 (ii) 1000 -110000 (iii) 110101 -10000

11.Give full form for following abbreviations and explain: (i) ASCII

(ii) EBCDIC

12.Explain weighted binary codes with examples.

13.Find 1’s and 2’s complement of following binary nos. (10001.101)2 (ii) (101011.11101)2

14.Find 9’s and 10’s complement of following binary nos.

3405.65,87.76

**ASSIGNMENT-2**

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**(Chapter-2- MINIMIZATION TECHNIQUES)**

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1. Given Boolean function is :

F= x y + x′ y′ + y′ z

a. Implement it with only OR & NOT gates

b. Implement it with only AND & NOT gates

2. Express following Function in Product of Maxterms form:

F(x,y,z)= ( xy + z ) ( y + xz )

3. Explain briefly : SOP & POS , minterm & maxterm , canonical form , propagation delay, fan out

4. What is the principle of Duality Theorem?

5. Explain briefly: standard SOP and POS forms.

6. What are Minterms and Maxterms?

7. Define: Noise margin , Propagation delay

8. Reduce the expression:

a. A+B(AC+(B+C’)D) b. (A+(BC)’)’(AB’+ABC)

9. Define : Integrated Circuit and briefly explain SSI, MSI, LSI and VLSI

10. Draw the logic symbol and construct the truth table for each of the following . [1] Two input NAND gate [2] Three input OR gate [3] Three input EX-NOR gate [4] NOT gate

11. Give classification of Logic Families and compare CMOS and TTL Families

12. Demonstrate by means of truth tables the validity of the following Theorems of Boolean algebra

(i) De Morgan’s theorems for three variables

(ii) The Distributive law of + over-

13. Express following functions in sum of min terms and product of max terms:

a. F(A,B,C,D) = D(A’+B) + B’D

b. F(A,B,C) = (A’+B) (B’+C)

c. F(x,y,z) = 1

**ASSIGNMENT-3**

**Subject Name: DIGITAL ELECTRONICS**

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**Chapter-2- MINIMIZATION TECHNIQUES**

**(Simplification of Boolean Function using K-Map)**

1. Simplify following Boolean function using K-Map and implement it with only

NAND gates.

F=A′B′C′+B′CD′+A′BCD′+AB′C′

2. Simplify following Boolean function using 4 variable K-Map.

F = Σ (0, 1, 2, 8, 10, 11, 14, 15)

3. Simplify following Boolean function using K-map and implement with only NOR

gates.

F( w,x,y,z) = Σ( 1 , 3 , 7 , 11 , 15 )

with don’t care conditions d( w,x,y,z ) = Σ( 0, 2 ,5 )

4. Simplify following Boolean function using K-Map Method

F(w,x,y,z ) = Σ( 0 ,1 , 2 , 8 ,10 ,11,14,15 )

5. Simplify Boolean function and draw logic diagram for simplified Boolean function:

(1)F(w,x,y,z) = Σ (0,1,2,4,5,6,8,9,12,13,14)

(2)F(w,x,y) = Σ (0,1,3,4,5,7)

6. Simplify Boolean function:

(1) F = A’B’C’+B’CD’+A’BCD’+AB’C’

(2) F =A’B’D’+A’CD+A’BC

d=A’BC’D+ACD+AB’D’ Where “d ” indicates Don’t care conditions.

7. Obtain simplified expressions in sum of products form for following Boolean functions and draw logic diagram for simplified expressions:

(i) *F*(A,B,C,D,E) =Σ(0,1,4,5,16,17,21,25,29)

(ii) A′B′CE′ + A′B′C′D′ +B′D′E′ + B′C D′

8. Simplify Boolean function F ( w,x,y,z ) = Σ ( 0,1,2,4,5,6,8,9,12,13,14 ) using K-map and

Implement it using (i) NAND gates only (ii) NOR gates only

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**ASSIGNMENT-4**

**Subject Name: DIGITAL ELECTRONICS**

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**(Chapter-3- Combinational Circuit Design**)

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**1.** Design Combinational Circuits for Binary to Gray Code Conversion.

**2.** Explain Design Procedure for Combinational Circuit & Difference between Combinational

Circuit & Sequential Circuit.

**3.** Construct 4\*16 Decoder with help of 2\*4 Decoder.

**4.** Discuss 4 bit BCD Adder in Detail.

**5.** Explain 4 bit Magnitude Comparator.

**6.** Explain common cathode type’s seven segments displays.

**7.** Design combinational circuits for a full adder.

**8.** Design a full-adder with two half-adders and an OR gate.

**9.** Design a combinational circuit for a full subtractor.

**10.** Design combinational circuits for a half adder.

**11.** Design a combinational circuit for a half subtractor.

**12.** Design a combinational circuit whose input is a four bit number and whose Output is the 2’s

Complement of the input number.

**13.** Draw symbol and truth table for four input EX-OR and EX-NOR gate. Explain NAND and

NOR as a universal gate.

**14.** Design BCD to Excess-3 code converter using minimum number of NAND gates.

**15.** Explain working of 4-bit binary parallel adder.

**16.** What is meant by multiplexer ? Explain with diagram and truth table the Operation of 4-to-1 line multiplexer.

**17.** What is meant by decoder ? Explain 3-to-8 line decoder with diagram and truth table.

**18.** Draw symbol and construct the truth table for three input Ex-OR gate.

**19.** Implement Boolean expression for Ex-OR gate using NAND gates only.

**20.** Design a BCD to decimal decoder.

**21.** Design a 4 bit binary to BCD code converter.

**22.** Design a full adder circuit using decoder and multiplexer.

**23.** Define: [1] Comparator [2] Encoder [3] Decoder [4] Multiplexer [5] De-multiplexer

**24.** Design a combinational circuit that accepts a three bit binary number and generates an output

binary number equal to the square of the input number.

**25.** Design a combinational circuit that generates the 9′ complement of a BCD digit.

**26.** Design a combinational circuit for 3-input parity generator and parity checker.

**ASSIGNMENT-5**

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**(Chapter-4- SEQUENTIAL CIRCUIT )**

1. Define Flip flop and explain basic function of it.

2. Draw and explain the working of following flip-flops

[1] Clocked RS [2] T-flip-flop

3. Draw logic diagram , graphical symbol , and Characteristic table for clocked D flip-flop

4. Discuss D-type edge- triggered flip-flop in detail.

5. Explain J-K flip-flop with necessary logic diagram, state equation and Truth table. How JK flip-flop is the refinement of RS flip-flop?

6. What is race-around condition in JK flip-flop?

7. Explain Master Slave Flip Flop through J.K Flip Flop with necessary logic diagram, state equation and state diagram.

8. Design Sequential Circuit with J.K. Flip Flops to satisfy the following state equation.

A( t + 1 ) =A′ B′ CD + A′ B′ C + ACD +AC′ D′ B(t+1)= A′ C + CD′ + A′ BC′ C(t + 1) = B D(t +1)=D′

9. Give classification of counters and explain asynchronous 4-bit binary ripple counter. Explain the count sequence. How up counter can be converted into down counter?

10. Explain 4-bit up-down binary synchronous counter.

11. Explain the procedure followed to analyze a clocked sequential circuit with suitable example.

12. Define: state table, state equation, state diagram, input & output equations.

13. Design a counter with the following binary sequence: 0, 4,2,1,6 and repeat. Use JK flip-flops.

14. Design a counter with the following binary sequence:0,1,3,7,6,4,and repeat.(Use T flip-flop)

15. Draw the state diagram of BCD ripple counter, develop it’s logic diagram, and explain it’s operation.

16. Construct a Johnson counter with Ten timing signals.

17. Design sequential counter as shown in the state diagram using JK flip-flops

**ASSIGNMENT-6**

**Subject Name: DIGITAL ELECTRONICS**

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**(Chapter-6 SEMICONDUCTOR MEMORIES AND PROGRAMMABLE LOGIC DEVICES)**

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1. Introduction to PLD and its types.

2. Compare RAM, ROM and EPROM.

3. Compare PLA and PAL.

4. Write short note on Programmable Logic Arrays.

5. Write short note on State machine on a Chip.

6. What is FPGA? Explain its basic structure.

7. A combinational circuit is defined by functions:

F1 (A, B, C) = Σ (3, 5, 6, 7) F2 (A, B, C) = Σ (0, 2, 4, 7) Implement the circuit with PLA having three inputs, four product term and two outputs.

8. Using the simplified connection format of PLA, Show how an 8×1 PROM should be programmed to implement the logic function

F (A, B, C) = Σ (1, 4, 5, 7)

9. Show how the PLA would be programmed to implement the functions. PLA having three inputs, four product term and two outputs.

F1=A(BC)’+ABC F2=ABC+(AB)’+AC’

10. Using the simplified connection format of PLA, Show how an 8×1 PROM should be programmed to serve as a look-up table for the odd parity-bit of a 3 bit number? Use the simplified connection format of PLA.

11. Show how the FPLA Circuit would be programmed to implement

F1= A’BC’+B’C+ABC

12. Implement the state diagram shown in fig. using PLS (Programmable Logic Sequencer )

100001110/10/10/11/01/01/01/00/0